**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of the Claims:**

1. (Currently Amended) A circuit comprising:

a signal input coupled to receive a signal;

a buffer circuit coupled to receive the signal input and to generate a buffer circuit output; and

a voltage following circuit comprising a first amplifier coupled to a first transistor and a second amplifier coupled to a second transistor, the voltage following circuit coupled to receive the signal input and to generate a voltage following output wherein the buffer circuit output and the voltage following circuit output are coupled to a circuit output node,

wherein the first amplifier comprises a positive input, a negative input and an output, and the first transistor comprises an NMOS transistor including a gate, a source and a drain, the positive input of the first amplifier being coupled to receive the input signal, the negative input of the first amplifier being coupled to the source of the NMOS transistor, the output of the first amplifier being coupled to the gate of the NMOS transistor, the drain of the NMOS transistor being coupled to a positive supply voltage, and the source of the NMOS transistor being coupled to the circuit output node, and

wherein the second amplifier comprises a positive input, a negative input and an output, and the second transistor comprises a PMOS transistor, including a gate, a source and a drain, the positive input of the second amplifier being coupled to receive the input signal, the negative input of the second amplifier being coupled to the source of the PMOS transistor, the output of the second amplifier being coupled to the gate of the PMOS transistor, the drain of the PMOS

transistor being coupled to a supply voltage less than the positive supply voltage, and the source of the PMOS transistor being coupled to the circuit output node.

2. (Canceled)

3. (Currently Amended) The circuit of claim ~~2~~ 1 wherein the positive input of the first amplifier is coupled to the signal input through a first output level based buffer impedance modulator circuit and the positive input of the second amplifier is coupled to the signal input through a second output level based buffer impedance modulator circuit.

4. (Currently Amended) The circuit of claim 1 wherein ~~the voltage following circuit comprises~~ the first transistor comprising an NMOS transistor including a gate, a source and a drain, the gate being coupled to ~~receive the input signal~~an output of the first amplifier, the drain being coupled to a positive supply voltage, and the source being coupled to the circuit output node, and

the second transistor comprising a PMOS transistor including a gate, a source and a drain, the gate being coupled to ~~receive the input signal~~an output of the second amplifier, the drain being coupled to a supply voltage less than the positive supply voltage, and the source being coupled to the source of the NMOS transistor and the circuit output node.

5. (Canceled)

6. (Original) The circuit of claim 1 wherein the circuit is part of a signal distribution system.

7. (Previously Presented) The circuit of claim 6 wherein the circuit is a repeater circuit in the signal distribution system.

8. (Previously Presented) The circuit of claim 6 wherein the circuit is a second buffer circuit at a distribution junction of the signal distribution system.

9. (Original) The circuit of claim 1 wherein the circuit is part of a large scale integrated circuit.

10. – 18. (Canceled)

19. (Currently Amended) A system comprising:

a microprocessor comprising a circuit including

a signal input coupled to receive a signal;

a buffer circuit coupled to receive the signal input and to generate a buffer circuit output; and

a voltage following circuit comprising a first amplifier coupled to a first transistor and a second amplifier coupled to a second transistor, the voltage following circuit coupled to receive the signal input and to generate a voltage following output wherein the buffer circuit output and the voltage following circuit output are coupled to a circuit output node,

wherein the first amplifier comprises a positive input, a negative input and an output, and the first transistor comprises an NMOS transistor including a gate, a source and a drain, the positive input of the first amplifier being coupled to receive the input signal, the negative input of the first amplifier being coupled to the source of the NMOS transistor, the output of the first amplifier being coupled to the gate of the NMOS transistor, the drain of the NMOS transistor being coupled to a positive supply voltage, and the source of the NMOS transistor being coupled to the circuit output node, and

wherein the second amplifier comprises a positive input, a negative input and an output, and the second transistor comprises a PMOS transistor, including a gate, a source and a drain, the

positive input of the second amplifier being coupled to receive the input signal, the negative input of the second amplifier being coupled to the source of the PMOS transistor, the output of the second amplifier being coupled to the gate of the PMOS transistor, the drain of the PMOS transistor being coupled to a supply voltage less than the positive supply voltage, and the source of the PMOS transistor being coupled to the circuit output node.

20. (Canceled)

21. (Currently Amended) The ~~circuit~~ system of claim 19 wherein ~~the voltage following circuit comprises~~ the first transistor ~~comprising~~ comprises an NMOS transistor including a gate, a source and a drain, the gate being coupled to receive the input signal, the drain being coupled to a positive supply voltage, and the source being coupled to the circuit output node, and

wherein the second transistor ~~comprising~~ comprises a PMOS transistor including a gate, a source and a drain, the gate being coupled to receive the input signal, the drain being coupled to a supply voltage less than the positive supply voltage, and the source being coupled to the source of the NMOS transistor and the circuit output node.

22. – 25. (Canceled)

26. (New) The system of claim 19 wherein the positive input of the first amplifier is coupled to the signal input through a first output level based buffer impedance modulator circuit and the positive input of the second amplifier is coupled to the signal input through a second output level based buffer impedance modulator circuit.

27. (New) The system of claim 19 wherein the system is part of a circuit distribution system.

28. (New) The system of claim 27 wherein the circuit is a repeater circuit in the signal distribution system.

29. (New) The system of claim 27 wherein the circuit is a second buffer circuit at a distribution junction of the signal distribution system.

30. (New) The system of claim 19 wherein the circuit is part of a large scale integrated circuit.